REMARKS

These remarks are in response to the Office Action mailed July 27, 2006 (Office Action). As this reply is timely filed, no fee is believed due. No new matter has been introduced.

In the Office Action, claims 6 and 11 have been objected to over minor informalities. Applicants have amended claims 6 and 11 in the manner suggested. Those skilled in the art will appreciate that the amendments to claims 6 and 11 have been made only to correct minor informalities. Accordingly, withdrawal of the objection to claims 6 and 11 is respectfully requested.

Claims 1, 3, 9, 16, and 18 have been rejected under 35 U.S.C. § 112, second paragraph. The phrase "regularly" has been removed from claims 1, 3, 16, and 18. With respect to claim 6, the phrase "the list containing object names for all used instances" has been amended to recite "the list containing object names for used objects", which is supported in independent claim 1. With respect to claim 9, the phrase "a repeated listed of root objects" has been amended to recite "a list of repeated root objects". With respect to claim 11, the phase "all used instances" has been amended to recite "all used objects", which finds antecedent basis within claim 11. In view these amendments, withdrawal of the 35 U.S.C. § 112, second paragraph, rejection of claims 1, 3, 9, 16, and 18 is respectfully requested.

Claims 1-13 and 16-20 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,345,378 to Joly et al. (Joly) in view of U.S. Patent No. 6,374,205 to Kuribayashi et al. (Kuribayashi). The Office Action contends that Joly teaches or suggests each limitation of independent claims 1, 16, and 18, with the exception of the step of "simulating the modified netlist". Applicants respectfully disagree. Applicants interpret the reference to "Joey" as "Joly".

Independent claims 1, 16, and 18 recite the limitations that "form a list of unused objects in the target architecture" and "replace at least one object in the list of unused objects with an appropriate dummy object," which are not taught or suggested individually or in combination by Joly or Kuribayashi. In contrast, Joly discloses a system in which cells from a gate level description of a netlist are selectively removed.

From the description in Joly, it is clear that "used" modules, as opposed to unused objects, are modified.

In illustration, the abstract of Joly states:

> This gate level description is reduced by removing internal gates to produce a synthesis shell of the synthesized block. The synthesis shell preserves input load and fanout for the block, output delay relative to clock for the block, setup / hold constraints on input signals relative to the clock for the block, and delay from input to output for pass through signals for the block. Such a synthesis shell can be used as a substitute for original design netlists . . . .

The passage indicates that Joly is altering blocks of a netlist that are used. In particular, Joly states that "setup / hold constraints on input signals relative to the clock for the block" are preserved, which clearly indicates that such blocks are being used. Thus, Joly not only fails to teach or suggest the limitations of independent claims 1, 16, and 18, but actually teaches away from the Applicants' invention. Claims 1, 16, and 18 recite that unused objects in the target architecture are replaced with dummy objects, while Joly teaches that selected cells of used blocks are deleted.

Kuribayashi suffers from the same deficiencies as Joly, it does not teach or suggest that unused objects in the target architecture are replaced with dummy objects. In particular, Kuribayashi selectively removes components from a circuit design without reference to whether the component is unused, in an effort to reduce the overall number of components. Applicants also note that, with regard to independent claims 1, 16, and 18, Kuribayashi has been cited only for teaching "the step of simulating the modified netlist", and not for teaching or suggesting any of the other limitations of these claims. Accordingly, neither Joly nor Kuribayashi, nor any combination thereof teaches or suggests Applicants' invention as recited in claims 1, 16, and 18.

With respect to claim 11, Joly has been cited for teaching the limitation of "emptying the repeated objects found on the list of repeated objects forming a plurality of dummy objects". Claim 11 further recites the step of "replacing any object in the netlist with a corresponding dummy object from the plurality of dummy objects if the object in the netlist is not on the list containing object names for all used objects to

form the modified netlist". Thus, the Applicants' invention replaces objects that are not on the list of object names for used objects, thereby replacing unused objects. These unused objects are replaced with the emptied objects. The objects can be replaced with emptied objects since the objects are not used in the target architecture.

By comparison, Joly selectively deletes cells, but does not empty a module. Emptying a module would result in a loss of functionality for that module, which Joly takes great care not to do. As neither Joly, Kuribayashi, nor any combination thereof teaches or suggests replacing unused objects, neither reference, taken independently or in combination, teaches or suggests the limitations of claim 11.

Claims 8 and 12 teach the step of "feeding through a signal unchanged when simulating the appropriate dummy object during a simulation process using the modified netlist". Because Joly preserves attributes of a block, such as output delay as noted herein, Joly does not pass a signal through unchanged. Rather the signal is changed as the signal passes through the modified block as would have occurred had the block not be modified by deleting one or more cells. Accordingly, Joly does not empty a module as recited in Applicants' claims.

Similarly, claims 10 and 13 recite that replacing includes "emptying a hardware description language version of a repeated object to form an object devoid of an explicit function mapping of an input to an output". Again, Joly does not empty a module, but rather selectively deletes cells of the module.

Relying in part upon Joly and Kuribayashi, claims 14 and 15 also have been rejected under 35 U.S.C. § 103(a). Accordingly, the remarks made in support of claims 1, 11, 16, and 18 are applicable here. While claims 14 and 15 are believed to be allowable on their own merits, both claims are allowable by virtue of their dependency upon independent claim 11.

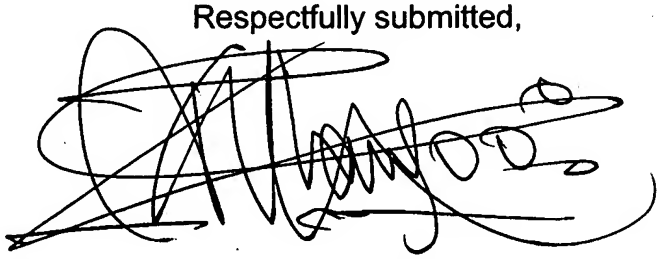
As neither Joly, Kuribayashi, nor any combination thereof teaches or suggests the Applicants' invention as claimed, withdrawal of the 35 U.S.C. § 103(a) rejection with respect to claims 1-20 is respectfully requested.

CONCLUSION

All claims should be now be in condition for allowance and a Notice of Allowance is respectfully requested.

If there are any questions, the Applicants' attorney can be reached at Tel: 408-879-7710.

Respectfully submitted,



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I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450, on October 11, 2006.

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